REMARKS

No claims have been amended. Claims 46-47 have been canceled. No new claims have been added. Claims 1-17, 19-22, 24-33, 35-41, 43-44, 48-49, and 51 are pending.

Applicant's representative is grateful for the allowance of claims 7-10, 14-17, 19-21, 28-31, and 36-39.

Claims 1-6, 11-13, 22, 24-27, 33, and 35 stand rejected under 35 U.S.C. § 102(a) as being anticipated by CPP (Cambridge Parallel Processing Gamma II Plus Technical Overview). This rejection is respectfully traversed.

Claims 1 and 22 recite, *inter alia*, "a circuit coupled between said main memory and said plurality of processing elements, wherein said circuit is adapted for: writing data from said plurality of processing elements to said memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements" (emphasis supplied).

Claim 11 and 33 recite, *inter alia*, " a plurality of data path circuits, each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements ... wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main memory in a horizontal mode, and to receive data stored in said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time" (emphasis supplied).

CPP discloses the Gamma II Plus series of computers, which, as illustrated in Fig. 2.1, includes a Master Control Unit (MCU) coupled to a code store. The MCU is

also coupled, in parallel, to a plurality of processor elements (PEs) which are organized to form a processor array. Each PE includes a 1-bit processor and a 8-bit processor. Each PE is also associated, via a direct connection, with a portion of an array memory. See CPP at page 2-10 ("Each PE has a one-bit wide, direction connection to its own section of the array memory.")

Fig. 2.1 shows no circuits coupled between any PE and its respective portion of the array memory. Accordingly, CPP cannot disclose or suggest any circuit or circuits which is/are "coupled between said main memory and said plurality of processing elements" as recited in claims 1, 11, 22, and 33.

The Office Action states at page 13 that the "processor array may be directly coupled to the array memory ... but this does not preclude the MCU from being coupled between the PE's and the memory array." This conclusion is in error, as the processor array is in fact (i.e., not merely "may be") directly coupled to the array memory. See CPP at Fig. 2.1 and page 2-10. Further, Fig. 2.1 clearly shows that the MCU is not coupled between any PE and any portion of the array memory.

The Office Action alleges at page 13 that the MCU may be "coupled between said main memory and one of said plurality of processing elements" by relying upon the assertion that Fig. 2.6 "clearly shows that the MCU is coupled to the data array through its Array Support Unit." In fact, as demonstrated below, Fig. 2.6 shows otherwise.

The MCU is the control unit which coordinates and controls the processing activities of the PEs. That is, the MCU distributes the code from the code store for execution by the PEs. As code is primarily comprised of instructions, the MCU is "... mainly concerned with issuing instruction streams to the" PE array. CPP, at page 2-11.

More specifically, Fig. 2.6 shows that instructions for the 8-bit processors of the PEs are issued via the CPAL Sequencer Unit, and instructions for the 1-bit processors are issued via the Array Interface. CPP further states that the Array Support Unit (ASU) performs the equivalent function with respect to array data as the Array Interface. CPP at page 2-13.

If the Array Interface and ASU are performing equivalent functions, but differ only with respect to the communication of instructions (Array Interface) and data (ASU), the object of the communication must also be equivalent. That is, the ASU must be communicating data to the PEs and not the array memory. This is further supported by Fig. 2.1, which fails to show any mechanism coupling the MCU with the array memory. Plainly put, there is no disclosure or suggestion in CPP that the MCU is coupled between the PEs and the array memory. As such, CPP cannot disclose or suggest the above quoted portions of independent claims 1, 11, 22, and 33.

Claim 32, 40-41, 43-44, 46-49, and 51 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Fung (U.S. Patent No. 4,380,046). This rejection is respectfully traversed.

Claims 32 and 40 recite, *inter alia*, "wherein said processing unit and said active memory device are on a same chip."

Claim 41 recites, *inter alia*, "wherein said data circuit passes said data directly to said memory device in a horizontal mode and ... wherein said circuit is further adapted to pass at least a portion of said data to said memory device in a vertical mode."

Claim 48 recites, *inter alia*, "wherein at least a portion of said data is stored in said memory device in a vertical mode."

Fung is directed to a massively parallel processor computer 20, which, referring to Fig. 1, comprises an array 22 of processing elements 44. The array 22 of processing elements 44 is provided instructions by an array control unit 24, while data flow is controlled by a program and data management unit (PDMU) 26. Fig. 2 is a more detailed illustration of each processing element 44, which comprises a processing element portion in the form of an arithmetic logic and routing unit (ALRU) 46. The ALRU 46 is coupled in parallel via signal path 52 to an I/O Unit 48 and a local memory unit 50.

With respect to dependent claims 32 and 40, the Office Action cites to column 5, lines 41-44, which state: "Thus, a considerable number of the processing elements 44 (approximately four, using present technology) can be fabricated on a single LSI chip." Fung therefore discloses that the array 22 of processing elements can be fabricated on a single chip. However, claims 32 and 40 require both the processor (i.e., a main processor) and an active memory device (i.e., a processing array with memory combination) to be on a same chip. Fung does not disclose or suggest such a feature. Accordingly, claims 32 and 40 are believed to be allowable over the prior art of record.

With respect to claims 41 and 48, each of these claims recite the use of a vertical mode of storage. The massively parallel processor 20 of Fung is incapable of storing data in a vertical mode, as each processing element 44 naturally stores data to its local memory unit 50 in a horizontal mode. Further, the I/O units 48, as illustrated in Fig. 3, are only capable of passing information horizontally. See also column 6, lines 40-42. Accordingly, Fung cannot be fairly stated to disclose or suggest "wherein said data circuit passes said data directly to said memory device in a horizontal mode and ... wherein said circuit is further adapted to pass at least a portion of said data to said memory device in a vertical mode" (as recited in claim 41) or "wherein at least a

portion of said data is stored in said memory device in a vertical mode" (as recited in claim 48).

Accordingly, independent claims 1, 11, 22, 33, 41, and 48 are believed to be allowable over the prior art of record. The depending claims (i.e., claims 2-6, 12-13, 24-27, 32, 35, 40, 43-44, and 49-51) are believed to be allowable for at least the same reason as the independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: October 21, 2004

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Christopher S. Chow
Registration No.: 46,493
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant